Amendments to the Claims

The following listing of claims replaces all previous claim listings and versions.

Claims 1-20 (Canceled)

21. (Currently Amended) An apparatus to generate a pulse width modulated voltage signal, said apparatus comprising:

a DC voltage source;

a first switching circuit comprising a first switch and a second switch configured in a series circuit, said first switching circuit electrically coupled in parallel with said DC voltage source;

a second switching circuit comprising a third switch and a fourth switch configured in a series circuit, said second switching circuit electrically coupled in parallel with said DC voltage source;

an output comprising a first electrical junction coupling said first switch with said second switch and a second electrical junction coupling said third switch with said fourth switch;

said second switching circuit configured to maintain said third switch in a conduction state while said fourth switch is maintained in a non-conducting state so as to establish a first polarity of an output signal;

said first switching circuit configured to switch said first switch and said second switch at a modulation frequency;

said first switching circuit configured to maintain said second switch in a conducting state while maintaining said first switch in a non-conducting state so as to establish a second polarity of said output signal, said second polarity being the reverse polarity of said first polarity; [[and]]

said second switching circuit configured to switch said third switch and said fourth switch at said modulation frequency; and

a microprocessor electrically coupled to the first and second switching circuits, wherein the microprocessor generates control signals according to a selected pulse width modulation scheme to control the timing and operation of the first and second switching circuits.

22. (Original) The apparatus as described in claim 21 wherein said first switching circuit and said second switching circuit are configured as part of an application specific integrated circuit.

23. (Previously Presented) The apparatus as described in claim 21 wherein said first switching circuit is configured to produce a positive pulse width modulated output signal during about one half cycle of a fundamental output period; and

wherein said second switching circuit is configured to produce a negative pulse width modulated output signal during the other half cycle of said fundamental output period.

24. (Original) The apparatus as described in claim 21 and further comprising a motor electrically coupled to said output.

25. (Canceled)

26. (Currently Amended) A method of generating a pulse width modulated voltage signal, said method comprising:

providing a DC voltage source;

electrically coupling said DC voltage source in parallel with a first switching circuit comprising a first switch and a second switch configured in a series circuit;

electrically coupling said DC voltage source in parallel with a second switching circuit comprising a third switch and a fourth switch configured in a series circuit;

establishing an output comprising a first electrical junction coupling said first switch with said second switch and a second electrical junction coupling said third switch and said fourth switch;

generating control signals with a processor according to a selected pulse width modulation scheme to control the timing and operation of the first and second switching circuits;

maintaining said third switch in a conduction state while maintaining said fourth switch in a non-conducting state according to the control signals so as to establish a first polarity of an output signal;

switching said first switch and said second switch at a selected modulation frequency; then

maintaining said second switch in a conducting state while maintaining said first switch in a non-conducting state according to the control signals so as to establish a second polarity of said output signal, said second polarity being the reverse polarity of said first polarity; and

switching said third switch and said fourth switch at said selected modulation frequency.

27. (Original) The method as described in claim 26 and further comprising:

configuring said first switching circuit and said second switching circuit as part of an application specific integrated circuit.

28. (Original) The method as described in claim 26 and further comprising:

utilizing said first switching circuit to produce a positive pulse width modulated output signal during about one half cycle of a fundamental output period; and

utilizing said second switching circuit to produce a negative pulse width modulated output signal during the other half cycle of said fundamental output period.

29. (Original) The method as described in claim 26 and further comprising powering a motor with said output signal.

30. (Canceled)